Research article

Yiwei Xie, Leimeng Zhuang* and Arthur J. Lowery

Picosecond optical pulse processing using a terahertz-bandwidth reconfigurable photonic integrated circuit

https://doi.org/10.1515/nanoph-2017-0113
Received November 16, 2017; revised January 23, 2018; accepted February 12, 2018

Abstract: Chip-scale integrated optical signal processors promise to support a multitude of signal processing functions with bandwidths beyond the limit of microelectronics. Previous research has made great contributions in terms of demonstrating processing functions and device building blocks. Currently, there is a significant interest in providing functional reconfigurability, to match a key advantage of programmable microelectronic processors. To advance this concept, in this work, we experimentally demonstrate a photonic integrated circuit as an optical signal processor with an unprecedented combination of two key features: reconfigurability and terahertz bandwidth. These features enable a variety of processing functions on picosecond optical pulses using a single device. In the experiment, we successfully verified clock rate multiplication, arbitrary waveform generation, discretely and continuously tunable delays, multi-path combining and bit-pattern recognition for 1.2-ps-duration optical pulses at 1550 nm. These results and selected head-to-head comparisons with commercially available devices show our device to be a flexible integrated platform for ultrahigh-bandwidth optical signal processing and point toward a wide range of applications for telecommunications and beyond.

Keywords: integrated optics; photonic integrated circuit; picosecond pulse processing; waveguide.

1 Introduction

Optical pulses are essential in many optical systems and have applications across different fields such as telecommunications, sensing, imaging and metrology [1–3]. The processing of optical pulses shares some commonalities with digital signal processing of electrical samples. A variety of optical pulse processing functions can therefore be synthesized by different combinations of optical components such as splitters, combiners and delay lines [4, 5].

The advance in photonic integrated circuit (PIC) technologies has enabled the implementation miniaturization of optical components [6–16]. PICs can be controlled accurately and are stable. Regarding integrated optical signal processors using PICs, previous research has made great contributions in terms of circuit design and implementing various processing functions, with a wide range of applications having been demonstrated [17–24]. The constant development of essential components and building blocks such as splitters/combiners [25, 26], (de)multiplexers [23, 27], couplers [4, 7], delay lines [8, 28] and phase shifters [16, 22] have shown promising results of performance in terms of size, loss, bandwidth, coupling efficiency, control power consumption and fabrication accuracy. On the circuit level, a well-studied circuit topology is the arrayed waveguide grating router (AWGR) [29], which joins two slab couplers with an array of linearly incremental waveguide delays. AWGRs are able to perform \( M \times N \) Fourier transforms, and therefore, their use has been investigated in optical communication and spectroscopic systems [30, 31]. While AWGRs can be used as building blocks in more complex systems [32–35], their rigid topology limits their functional flexibility. In contrast, topologies comprising coupler arrays and delay lines offer design flexibility and easy incorporation of tuning elements [36–39]. A key advantage for signal processing is that these features support custom-synthesis of processing responses in both time and frequency domains, i.e. impulse responses and spectral responses. To date, a number of important functions have been demonstrated using such topologies,
including delay lines [40–42], temporal waveform shapers [24, 43], spectral filters [44–51], multi-port switches [52–56], Fourier transforms [23, 45], correlators [57], beamformers [58–61], quantum processors [62, 63] and mesh networks [64–66].

Although it has explored a wide diversity of functions, most of the previous research was directed toward engineering such devices for one particular function. This paradigm is inflexible, costly and risky, which slows their commercial adoption. It is therefore highly desirable for a photonic chip to be able to switch between different functions by means of programming and also can be tuned and optimized for post-production. This not only provides a path to significantly reducing the cost per function, but more importantly, one common verified design can be used for many applications [65, 67–69]. This concept has been successfully implemented in microelectronics, such as FPGAs and programmable digital processors [70]. The future adoption of PICs obviously also depends on whether they can provide adequate performance. In particular, the processing of picosecond optical pulses requires terahertz-processing bandwidths to guarantee the quality of the output signals. However, it is challenging to provide all these device features on a small chip area. High-index-contrast waveguides such as silicon on insulator and III-V semiconductors support very small bend radii for compact designs [7, 8]. However, currently, they still have significant propagation losses in the order of a few decibels per centimeter and a variation of propagation constant with wavelength. In addition, these waveguides also have strong nonlinear effects at high optical powers (e.g. >100 mW) [71, 72], which are detrimental to pulse processing. On the other hand, low-index-contrast waveguides such as silicon dioxide and silicon oxynitride provide good performance, but typically associate with larger device sizes [9, 12].

Here, we present a first demonstration of implementing a diversity of terahertz-bandwidth processing operations on picosecond optical pulses using an optical signal processor chip. This includes two binary-tree coupler arrays and an array of 16 delay lines with 6.25-ps differential delay. It is fabricated in stoichiometric silicon nitride Si₃N₄/SiO₂ waveguides on an area of 0.9 cm². The fiber-to-fiber insertion loss of the packaged chip is 5 dB at optimal coupling. In the experiments, we have verified that our processor chip is able to implement multiple and distinctively different processing functions, including terahertz-bandwidth clock rate multiplication, arbitrary waveform generation, discretely and continuously tunable delays, multi-path combining and bit-pattern recognition, for 1.2-ps-duration optical pulses at 1550 nm.

### 2 Device description

Figure 1 shows the optical signal processor chip fabricated using a Si₃N₄/SiO₂ waveguides [10, 14] (TriPleX, a proprietary waveguide technology of LioniX International). The design comprises three serial concatenated sections as depicted in Figure 1A: a binary-tree-structured 8 × 16 coupler array based on 2 × 2 tunable Mach-Zehnder interferometers (MZIs), a 16-arm array of linearly incremental delay lines with each arm equipped with a tunable phase shifter and an inter-arm delay interval of 6.25 ps and a binary-tree 16 × 8 coupler based on 3-dB directional...
couplers. The tuning elements are implemented thermooptically using chromium heaters. This architecture minimizes the circuit complexity and heat dissipation compared with designs using a parallel array of couplers (which require more building blocks and tuning elements), while guaranteeing full control of both amplitude and phase of each optical path (i.e. full control of complex coefficients, as in a spatial light modulator [73]). The fabricated chip is shown in Figure 1B, which has a chip area of 0.9 cm². As shown in the inset of Figure 1B, the waveguide uses a “double-stripe” geometry, i.e. two stripes of Si₃N₄ with a width of 1.2 μm, a thickness of 170 nm and a vertical spacing of 500 nm filled with SiO₂. This waveguide has a reported propagation loss of 0.15 dB/cm, group index of 1.71 and wavelength dependency of 2×10⁻⁵/nm [10, 14]. It supports a single mode at 1550 nm and is optimized for light coupling with TE polarization. The fully packaged chip is shown in Figure 1C, where all the heaters are wire-bonded to a carrier printed circuit board and optical I/Os are pigtailed with polarization-maintaining fibers.

More specifically, Figure 2 shows the chip layout. We used OptoDesigner (PhoeniX Software) to layout the chip. The design is a compromise between chip area, possible inter-component cross-talk and efficient routing of both optical and electrical paths. An S-shaped spiral with a bend radius of 150 μm is used for the delay lines to minimize the area. The 4-level binary-tree-structured coupler arrays are folded into a two-column layout. This layout guarantees two features for proper operation of the processor chip: (1) that all the couplers from the same stage of the binary tree are connected with equal lengths of waveguide to the other stages, so that the delay differences between optical paths in the circuit are only determined by the designated delay lines, and (2) that the tunable couplers are equally spaced in each column with a minimum spacing of 250 μm between a heater and a neighboring waveguide to minimize the thermal cross-talk between them. The heaters in the phase shifter section are equally apart with a spacing of 350 μm and are placed outside the delay spirals to minimize their impact on the areas dense with waveguides. Regarding the electrical paths, several considerations are taken into account. Two interconnected ground tracks with widths of 300 μm are used such that all heaters are able to connect to a ground track with a short lead so as to minimize electrical cross-talk as well as the current per ground track. The track width is 100 μm, to accommodate the current required for the full tuning range of each heater (each heater has 600 Ω resistance). Moreover, the circuit topology has test inputs and outputs, allowing access to different circuit sections independently, which simplifies device characterization and increases the operational flexibility.

3 Experimental results

3.1 Basic characterization

For the characterization of the circuit components, we chose the section between input 8 and output 8, as shown in Figure 1A, which comprises a simple bar-port delay interferometer with two arms (arms 1 and 2). The measured optical power responses at different heater biases of arm 2 are shown in Figure 3A. A bias power of 0.46 W is needed to generate a phase change of 2π in arm
resulting in a frequency shift of the optical response by an entire frequency spectral range (FSR). Figure 3B shows the extinction ratio (ER) as a function of the bias of the tunable coupler (MZI 15). The resulting ER is about 23 dB. The effects of thermal cross-talk are shown in Figure 3C and D. It is evident in Figure 3C that the null depth is insensitive to the cross-talk from the neighboring heaters (MZI 14 and MZI 7). Figure 3D shows the effect of cross-talk between heaters in arms 2 and 3 on arm 1, which results in an additional phase change and manifests as a frequency shift of the optical response. Owing to a sufficient inter-arm spacing in our design, the cross-talk effect is only about 3% between two neighboring arms and almost negligible for larger spacing. In practice, this effect can be compensated using the heater on the target arm.

For the control of the tuning elements, a custom 12-bit multi-channel voltage controller was used (LioniX International). In principle, automatic-control algorithms can be developed to drive the voltage controller for realizing automatic control, e.g. automatic translation from target functions into tuning element parameter settings [74]. However, in this work, the control for chip characterization and reconfiguration were performed manually with the parameter settings recorded in a look-up table. The difficulty of generating an auto-control algorithm lies mainly in the characterization of the initial offsets, tuning function to input and cross-talk between the tuning elements, which constitute a transfer matrix with the dimension of $N \times N$, with $N$ being the number of tuning elements on chip.

### 3.2 Terahertz-bandwidth optical clock rate multiplication

To date, integrated pulse train sources have been widely investigated in both academia and industry. For practical applications, switchable repetition rates are a desirable feature. However, this is inherently difficult to implement in many pulse sources due to a fixed cavity length. An effective way to overcome this drawback is to multiply the pulse repetition rate externally by means of modifying the optical spectrum of the pulse train signal using an optical filter. It is also desirable to implement such filters on chip with the lasing itself.

In this context, our processor chip can be configured to be a tapped delay line filter with a maximum of 16 taps, where middle input 4 and output 4 are used as optical I/Os. Mathematically, such a filter can be modeled as a digital finite impulse response filter [4], the transfer function of which is given by...
\[ H(f) = \frac{\Gamma}{N^r} \left[ \sum_{n=0}^{N-1} a_n e^{-j\phi_n} e^{-j2\pi f n} \right] \]

where \( f \) is the optical frequency, \( \Gamma \) is an amplitude normalization constant, \( N \) is the number of taps (arms) and \( \tau_n \) is the delay of tap \( n \). For the \( n \)th tap, the amplitude and phase coefficients are \( a_n \) and \( \phi_n \), respectively. These two coefficients can be varied by means of the tunable MZIs and phase shifters. This also provides on-off switching of each filter arm and enables filter passband shaping as well as frequency tuning.

Figure 4 shows a number of measured filter responses with respect to different coefficients. We used a Luna OVA5000, and a stopband null suppression of about 30 dB was achieved across the entire bandwidth of interest. The maximum FSR of the filter is determined by the inter-arm delay interval \( \tau = 6.25 \) ps by the relation \( f_{\text{FSR}} = \frac{1}{\tau} = 160 \text{ GHz} \). Figure 4A shows the filter response with all arms switched fully on \((a_n = 1)\) and phase-aligned \((\phi_j = \phi_k)\). A sinc response is expected. The relative error between the experimental and the theoretical response using Eq. (1) is around 5% due to the limited ER of the MZI couplers on the chip. Figure 4B demonstrates the frequency shifting of the filter passband without changing the passband shape. This was performed across a full spectral range, by adding a linearly incremental phase shift across all arms. Figure 4C and D demonstrates the tuning of the passband bandwidth and FSR. This was performed by tuning the amplitude coefficients of the filter, implemented by means of the tunable MZIs in the \( 1 \times 16 \) splitting circuit. The corresponding filter coefficient configurations are specified alongside for clarity.

The capability of defining both the passband repetition bandwidth and the frequency spacing between the stopband nulls is the key for implementing optical clock rate multiplication, where the filter passbands select the desired frequency components of the clock signal and the stopband nulls provide the maximum suppression to the undesired ones.

To verify the optical clock rate multiplication function [75], we configured our processor chip into two different tapped delay line filter topologies: \( \text{(A, B)} \) a 2-tap filter with a FSR of 20 GHz and \( \text{(C, D)} \) a 4-tap filter with a FSR of 40 GHz, by selectively switching on a number of...
arms. The measured filter responses optimized for equal-suppression stopband nulls are shown in Figure 5B and D, respectively. Figure 5A and C shows the spacing between the passband peaks. The measurements were performed with a bandwidth about 2.5 THz. A FSR variation smaller than 3% and stopband-null suppression larger than 30 dB.

Figure 5: Measured filter responses and FSR uniformity across a bandwidth of 2.5 THz: (A, B) for a 2-tap 20-GHz-FSR filter topology; (C, D) for a 4-tap 40-GHz-FSR filter topology. Measured signal spectra and waveform obtained from a PD: (E, F) input clock signal at 10 Gpulses/s; (G, H) output clock signal at 20 Gpulses/s; (I, J) output clock signal at 40 Gpulses/s.
were achieved across this bandwidth. Then, we applied an optical clock/periodic pulse train signal with a repetition rate of 10 Gpulses/s as the input. The corresponding optical spectrum and waveform obtained by a 70-GHz bandwidth photodetector (PD) and 62-GHz bandwidth real-time scope are shown in Figure 5E and F, respectively. The observed pulse width is about 20 ps. The filter output using the 2-tap 20-GHz-FSR filter topology is shown in Figure 5G and H, showing the spectrum and waveform of the output clock/pulse train signal, respectively. Evidently, the filter suppresses every other comb line in the spectrum, with a suppression ratio of 29 dB, and thereby changes the comb line spacing from 10 to 20 GHz. Concurrently, the pulse interval in the time domain reduces from 100 to 50 ps. This result shows an implementation of a doubling of the pulse repetition rate. The filter output using the 4-tap 40-GHz-FSR filter topology is shown in Figure 5I and J. Likewise, this result shows a quadrupling of the pulse repetition rate, where the filter suppresses three in every four spectral comb lines, resulting in a comb line spacing of 40 GHz and correspondingly a pulse interval of 25 ps. These demonstrations provide verifications of the function of a reconfigurable optical clock multiplier.

To further demonstrate the qualities of our output clock signal, we applied it in a PRBS-signal transmission experiment and made a head-to-head comparison with a reference implementation using a commercial optical clock multiplier based on free-space optics (PriTel optical clock multiplier). Using the chip and the commercial multiplier, respectively, we first generated 20- and 40-Gpulses/s clock signals from a seed clock signal at 10 Gpulses/s with a pulse duration of 1.2 ps, where both devices were optimized to provide maximum suppression to the undesired frequency components in the outputs. The outputs of the clock multipliers are fed to a 35-Gbits/s IQ modulator (TeraXion IQM, only one modulator is used), which are driven by a pulse pattern generator (SHF BPG 44E). For a clear comparison, Figure 6 shows the electrical spectra corresponding to their waveforms after detection. For both the 20- and 40-Gpulses/s cases, the filter chip demonstrates similar performance to the commercial multiplier, showing similar sidelobe suppression ratios, i.e. 35 dB for the 20-Gpulses/s case and 30 dB for the 40-Gpulses/s case. Then, we used these generated clock signals as the light source in a back-to-back transmission system. We externally modulated them with on-off keying with the symbol rates matched with the pulse repetition rates. As a performance indicator, the bit error rates (BER) versus optical signal-to-noise ratio (OSNR) of the received on-off keying signals were measured and compared, as shown in Figure 7A. The filter chip has a nearly identical BER performance to the commercial multiplier for both 20 and 40 Gpulses/s. To show the utility of these signals, Figure 7B also includes an optimal transmission case where the seed clock signal was generated using a commercial mode-locked laser (MLL) (Lumentum ERGO) at 10 Gpulses/s as a pulse source into the modulator. As shown in Figure 7B, the filter chip shows nearly no degradation to the signal.

### 3.3 Arbitrary waveform generation

Defining signal waveforms at high speeds is essential for modern telecommunications and radar systems, where large signal bandwidths are used. Conventional implementations of high-speed arbitrary waveform generators (AWG) require fast and power-hungry digital-to-analog converters. As the demand for signal bandwidth increases, it is challenging to provide all-electronic solutions. A state-of-the-art commercial AWG with a sampling rate about 100 GSa/s and an electrical bandwidth about 40 GHz is still too expensive to be adopted for applications out of the laboratory. However, photonic approaches open...
an alternative path for implementing high-speed AWGs with potential for low cost and power consumption.

To date, a number of photonic chip implementations of AWG have been reported with promising results [18, 32, 42]. One straightforward way to synthesize a particular electrical waveform is to use the time-domain impulse response of a tapped delay line filter. In this approach, the impulse response of the filter converts a short input pulse into a serial sequence of multiple pulses with their intensity envelop defined by the amplitude coefficient of each tap. Then, an according electrical waveform can be obtained by detecting this optical signal. As explained earlier, our processor chip can be configured to be a 16-tap delay line filter with a time-domain impulse response resolution of 6.25 ps, equivalent to an AWG sample rate of 160 GSa/s.

Figure 8 shows the synthesis of a number of representative waveforms from an input pulse with a duration of 2 ps, verifying the capability of arbitrary waveform generation. The corresponding filter coefficient configurations are specified for clarity. Figure 8A and B shows the waveforms of a falling ramp and a rising ramp, respectively. Figure 8C shows a triangular waveform. Figure 8D is a waveform showing height control of ramps and steps. Figure 8E shows a waveform having both climbing and falling steps. Figure 8F is a waveform approximating a sinc shape. Figure 8G is an approximation of a square waveform. Figure 8H shows a waveform of a random binary bit pattern. The filter configurations are shown in the inset table. These results provide a demonstration of the AWG with the waveforms directly synthesized in the time domain. In these results, the relative error between the simulation and theoretical results is less than 8%, the deviations from the ideal waveforms are mainly caused by six limiting factors: limited ER of the MZI couplers on the chip, limited bandwidths of PD and oscilloscope, limited noise floor of the optical amplifier, limited ER and finite time duration of the input optical pulses. In practice, these limitations should be taken into account for system design in accordance to the performance requirement. Some possible measures for improvement include, for example: using multi-stage MZI architectures with higher coupler ERs [56], reducing chip insertion loss [12], designing proper sample rate based on the electrical bandwidth, and using narrower and cleaner optical pulses as input [76].

3.4 Discretely and continuously tunable delays

Tunable delays are an essential building block for optical signal processors that perform signal timing control [42, 77]. Our processor chip is able to implement two types of tunable delay lines. Type 1 is with digitally switched tunability and a discrete delay steps. The other type, i.e. type 2, is with continuous variable delay.

For the implementation of type 1 delay line, the switching matrices on the chip perform as an end-to-end optical path selector routing the signal from the chip input (input 4 or 5) to output (output 4 or 5) with one of the 16 delays in its path. As such, the resulting delay line enjoys the terahertz-level bandwidth of the waveguide and features a delay tuning range from 0 to 93.75 ps, with a tuning step of 6.25 ps. Figure 9 shows the measured delay responses in the frequency domain, group delay (GD) and an experimental verification of its applicability to a narrow optical pulse with a duration of 1.2 ps, i.e. a bandwidth of 0.4 THz.

For the implementation of the type 2 delay line, the chip is configured to be an asymmetric MZI (A-MZI) comprising two adjacent delay spirals (e.g. arms 1 and 2), equivalent to a 2-tap delay line filter as explained earlier. In this case, the filter passband provides a delay value between those of the two spirals. This delay value can be continuously tuned by means of controlling the coupler

![Figure 7: BER measurements: (A) received on-off keying signals for the commercial optical clock multiplier and chip; (B) optimal transmission case for MLL and chip with different pulse repetition.](image-url)
Y. Xie et al.: Picosecond optical pulse processing using a terahertz-bandwidth reconfigurable PIC

However, as a trade-off with the continuous tunability, such a delay implementation has a bandwidth limitation as shown in Figure 10A, i.e. half of the filter FSR, which in our case is 80 GHz. Figure 10A and B illustrates the spectra and GD of different delay cases. Figure 10C shows the measured delay responses as a type 2 delay line and its corresponding timing control on a square pulse with a duration of 100 ps, equivalent to a pulse bandwidth about 10 GHz, which verifies its function. In a further experiment, the eye diagrams of a 10-Gbaud on-off-keying signal passing through the delay line was measured and shown in Figure 10D. It can be seen that the signal has clear eye opening over the entire delay tuning range of 93.75 ps, verifying the device performance uniformity and its applicability for optical communications. The delay value has little effect on the time jitter, showing an insignificant increase of 0.5% of the signal baud rate between the maximum minimum delays. This increase is mainly attributed to a higher ASE noise incurred during optical amplification.

3.5 Multi-path combining (optical time division multiplexing (OTDM))

Combining multiple inputs enables generation of a signal streams with high symbol rates by combining a number of signal tributaries with lower symbol rates. This technique benefits the transmission spectral efficiency and relaxes the electrical bandwidth requirement on modulators [78].

To demonstrate the multi-path combining function using our processor chip, we configured the input coupler matrix to be an array of four parallel equal-length routing paths, which then connect, respectively to four delay spirals with delay increments of 25 ps as shown in Figure 11A. After the delay section, the coupler matrix performs the combining and leads the combined signal to the middle output. This chip configuration is able to multiplex four pulse trains of 10 Gpulse/s into a 40-Gpulse/s stream. In the experiment, we split a 10-Gpulse/s, 1.2-ps-duration pulse train into four equal portions and time-aligned them at the chip inputs. The chip output was detected, and the resulting electrical waveform is shown in Figure 11B. This result shows a pulse train with a pulse interval of 25 ps, i.e. a pulse rate of 40 Gpulse/s, which verifies the combining function as designed.

3.6 Applications for optical communications

3.6.1 Nyquist-OTDM

“Orthogonal” time division multiplexing (OrthTDM) is based on interleaving $M$ modulated sinc pulses per TDM symbol. A practical application is to create a high-rate optical channel using lower-rate optical modulators [78].
In [79], we proposed a direct implementation of a near-Nyquist WDM filter, using an FIR with amplitude weighting of each of its waveguides to give a truncated-sinc (TS) impulse response. The filter is fed with OTDM pulses, and the output is Nyquist-OTDM signal. In this case, the reconfigurable filter is working as a FIR filter, considering the FSR of the filter and receiver speed limitation, we tuned the filter to have a near rectangular frequency response, with a nominal bandwidth, $B$, of 40 GHz and its impulse response is a truncated sinc with pulse width 25 ps, which can be expressed as [79]

$$h(t) = \text{sinc}\left(\frac{t - T_{\text{MLl}}/2}{\Delta T}\right) \text{rect}_{\frac{T_{\text{MLl}}}{2}}(t - T_{\text{MLl}}/2),$$  \hspace{1cm} (2)$$

where the rectangular function used here is

$$\text{rect}_{\frac{T_{\text{MLl}}}{2}}(t) = \begin{cases} 1 & 0 \leq t \leq T_{\text{MLl}}/2 \\ 0 & \text{otherwise} \end{cases},$$  \hspace{1cm} (3)$$

$T_{\text{MLl}}$ is the repetition rate of the MLL and $\Delta T$ is the pulse width of the truncated sinc. The reconfigurable filters have 16 arms with differential delays of $\Delta t = 6.25$ ps, giving a FSR of 160 GHz. The power in each arm of the filter can be calculated as

$$a_n = \frac{1}{A}\left(\text{sinc}\left(\frac{(n-1)\Delta t - T_{\text{MLl}}/2}{\Delta T}\right)\right)^2 \quad 1 \leq n \leq 16. \quad (4)$$

The FIR filter’s frequency response and waveform of the FIR filter with an input pulse with a duration of 1.2 ps are shown in Figure 12A and B. This filter is fed with OTDM pulses created by splitting, modulating, delaying then combining pulses from a MLL. Here, the MLL produces a train of short-pulses at 100-ps intervals and modulated with OOK at 10 Gbaud by an intensity modulator. The spectra before and after the chip are shown in Figure 12C; the modulated signals are shaped into near rectangular shapes by the FIR filter.
At the receiver, the Nyquist-OTDM signal is amplified and filtered by an 80-GHz Gaussian 1st-order BPF to remove energy from the higher-order passbands of the FIR filter. Figure 12D shows the signal quality for Nyquist-OTDM system when changing the OSNR and an open eye diagram at OSNR of 15 dB.

### 3.6.2 Optical bit pattern recognition

We further validate the operation of the correlator filter [57] by demonstrating all-optical recognition of 4-bit binary phase-shift-keyed (BPSK) patterns. This could be used to detect training identities, for example. Figure 13A shows the optical intensity waveform of a BPSK pattern input to the correlator. The input consists of four consecutive pulses at 40 Gpulse/s, with equivalently a delay interval of 25 ps between the pulses. The pulses are generated from a CW external cavity lasers (ECLs) and BPSK encoding is achieved by a modulator (TeraXion IQM, only one port is used). The phases of the input signal are encoded as $[0, \pi, 0, \pi]$. Our filter is configured such that only four arms are in use with their delay interval, amplitude and phase coefficients matching the input BPSK data amplitude.
Figure 13B–F are the auto-correlation signal of the BPSK signal with the correlator tuned to have phases of \([0, \pi, 0, \pi], [0, 0, 0, 0], [0, \pi, \pi, \pi], [\pi, \pi, 0, \pi] \) and \([0, 0, \pi, \pi]\). Here, the heights of the peaks, normalized with respect to the maximum auto-correlation peak in Figure 13B. We observe that the filter is capable of distinguishing the different patterns. The auto-correlation signals show the same features as the theoretically expected values (red dashed lines), with a relative error of around 7% because of the limited ER of the MZI couplers on the chip and limited bandwidths of PD and oscilloscope; further validating the correlator function. It is worth mentioning that in principle our filter design can recognize many other patterns, e.g. ASK and QPSK, on a maximum of 16 pulses spaced by 6.25 ps because of the full control of filter coefficients (i.e. amplitude and phase) in all 16 arms. However, the demonstration of this is beyond the speed limits of our measurement equipment.

4 Discussions and conclusions

We have shown a pathway toward the exciting prospect of reconfigurable optical signal processor chips. The PIC implementation also facilitates such devices to be integrated by means of micro-assembly with active circuit components such as lasers, modulators and photodiodes in one unit [80], opening a possibility for creating fully integrated, multi-purpose optical processing “engine” as a stand-alone device. Such processor chips enable variations of processing functions by means of electrical control, which features high accuracy as well as robustness, and implies potential for a wide range of applications.

The terahertz-bandwidth and low-loss properties of the silicon nitride waveguide allow processing of picosecond optical pulses as good as commercial counterparts based on free-space optics. Considering a future direction of development, ultrahigh-bandwidth processing on femtosecond pulses would open a new category of applications. In principle, the silicon nitride waveguide used in our work supports a transparent window from UV to near IR and has lower wavelength-dependency in terms of loss than silicon waveguide [14]. However, as an important performance aspect, signal processors based on interferometric circuits have their spectral repeatability (FSR uniformity) depending on the waveguide index variation and circuit parameter accuracy. The
The direction of effort for improvement lies mainly in the physical layer design of the waveguide and fabrication accuracy as well as uniformity, which requires in itself long-term development. On the circuit level, a challenge for the topology design is the delay accuracy of the optical paths in the processor. This would be a difficult task for ultrahigh-bandwidth applications, because different types of building blocks such as straights, bends, couplers and tuning elements may be included in different paths and each may introduce a waveguide index variation. Three practical methods may be considered to minimize the effect. One way is to use uniform layout of delay lines and introduce required delay differences only in the straights. The second is to use binary-tree coupler topology to implement equal-length splitters (combiners). The last is to try to route all delay lines across as much as possible the same regions on the wafer instead of distributed in different regions.

Figure 13: (A) Input signal amplitude with bit pattern \([0, \pi, 0, \pi]\). (B–F) Correlator outputs with correlator bit patterns (B) \([0, \pi, 0, \pi]\); (C) \([0, 0, 0, 0]\); (D) \([0, \pi, \pi, \pi]\); (E) \([\pi, \pi, 0, \pi]\) and (F) \([0, 0, \pi, \pi]\).
This work demonstrates reconfigurability using thermo-optical tuning mechanism. Further device development could consider electro-optical [11, 13], graphene-based [6] and stress-optical tuning mechanism [81] to lower power consumption and increasing tuning speed. Moreover, our circuit topology is also implementable in other waveguide materials. This means that further development may consider increasing device compactness as well as power efficiency and even the possibility of hybrid electronics-photonics integration using silicon technology platforms. Alternatively, monolithic integration of both passive and active circuit components using III-V semiconductor technology platforms would also bring desirable features and new capabilities to such devices. The demonstrated functions and comparisons with the commercially available devices underline not only versatile and high-performance manipulation of optical short pulses on the chip scale, but more significantly, a flexible integrated device platform for ultra-high-bandwidth optical signal processing.

Acknowledgments: This work is funded by the Australian Research Council under grants FL130100041 and CE110001018. We thank LioniX International, The Netherlands, for fabricating and packaging the test chip. We thank Ms Caterina Taddei with the Laser Physics and Nonlinear Optics (LPNO) group at the University of Twente, The Netherlands, for the chip quality check. We thank Binhuang Song from Monash University for the assistance in the experiments.

References


